CAT-5 Receiver with Adjustable Line Equalization

AD8128

FEATURES

- Tuned to compensate for Category-5 (CAT-5) cable losses
  - Up to 100 meters @ 120 MHz
- 2 voltage-controlled frequency response adjustment pins
  - High frequency peaking adjustment
  - Broadband gain adjustment
- 2700 V/µs slew rate
- Low output noise
  - 1.5 mV rms integrated noise (1 GHz) @ 100 meters equalized bandwidth
- DC output offset adjust
  - Low offset voltage error: 7 mV typ
- Equalized pass-band ripple ±1 dB to 70 MHz
- Input: differential or single ended
- Supply current: 24 mA on ±5 V
- Small 8-lead 3 mm × 3 mm LFCSP

FUNCTIONAL BLOCK DIAGRAM

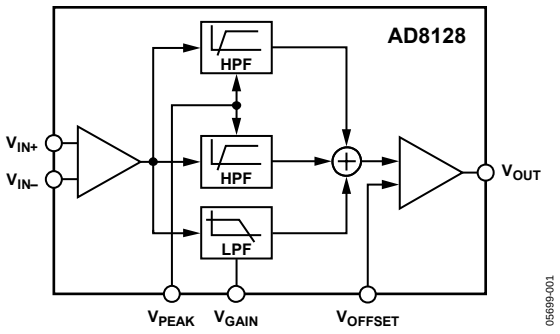

Figure 1.

APPLICATIONS

- Keyboard-video-mouse (KVM)
- RGB video over unshielded twisted pair (UTP) cable receivers
- Professional video projection and distribution
- Security video

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GENERAL DESCRIPTION

The AD8128 is a high speed, differential receiver/equalizer that compensates for the transmission losses of unshielded twisted pair (UTP) CAT-5 cables. Various frequency dependent gain stages are summed together to best approximate the inverse frequency response of CAT-5/CAT-5e cable. An equalized bandwidth of 120 MHz can be achieved for 100 meters of cable.

The AD8128 can be used as a standalone receiver/equalizer or in conjunction with the AD8143, triple differential receiver, to provide a complete low cost solution for receiving RGB over UTP cable in such applications as KVM.

The AD8128 has three control pins for optimal CAT-5/CAT-5e compensation. The equalized cable length is directly proportional to the voltage applied to the V_{PEAK} pin, which controls the amount of high frequency peaking. V_{GAIN} adjusts the broadband gain from 0 dB to 3 dB, compensating for the resistive cable loss. V_{OFFSET} allows the output to be shifted by ±2.5 V, adding flexibility for dc-coupled systems.

Low integrated output noise and offset voltage adjust make the AD8128 an excellent choice for dc-coupled wideband RGB-over-CAT-5 applications. For systems where the UTP cable is longer than 100 meters, two AD8128s can be cascaded to compensate for up to 200 meters of CAT-5/CAT-5e.

The AD8128 is available in a 3 mm × 3 mm 8-lead LFCSP and is rated to operate over the extended temperature range of −40°C to +85°C.

Rev. 0
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REVISION HISTORY

10/05—Revision 0: Initial Version

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SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Belden Cable, V_{OFFSET} = 0 V, V_{GAIN} and V_{PEAK} set to optimized settings (see Figure 4), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p, 100 meter CAT-5		120		MHz
±1 dB Equalized Bandwidth Flatness	V_{OUT} = 2 V p-p		70		MHz
Rise/Fall Time	V_{OUT} = 2 V step, 50 meter CAT-5		2		ns
Rise/Fall Time	V_{OUT} = 2 V step, 100 meter CAT-5		3.6		ns
Settling Time to 2%	V_{OUT} = 2 V step, 50 meter CAT-5		26		ns
Settling Time to 2%	V_{OUT} = 2 V step, 100 meter CAT-5		36.4		ns
Integrated Output Voltage Noise	V_{PEAK} = 0.9 V, V_{GAIN} = 225 mV, BW = 1 GHz		1.5		mV rms
DC PERFORMANCE					
Input Bias Current			15.5	24	µA
V_{OFFSET} Pin Current			1.7	8.2	µA
V_{GAIN} Pin Current			2	3.4	µA
V_{PEAK} Pin Current			4.2	6.8	µA
INPUT CHARACTERISTICS					
Input Differential Voltage			±2.8		V
Input Common-Mode Voltage			±3.0		V
Input Resistance	Common mode		380		kΩ
	Differential		675		kΩ
Input Capacitance			1.7		pF
Common-Mode Rejection Ratio (CMRR)	200 kHz, $\Delta V_{OUT}/\Delta V_{IN, cm}$	−63	−74		dB
ADJUSTMENT PINS					
V_{PEAK} Input Voltage	Relative to ground	0		1	V
Maximum Peak Gain	@ 120 MHz, V_{PEAK} = 1 V		20		dB
V_{GAIN} Input	Relative to ground	0		1	V
Maximum Broadband Gain	V_{GAIN} = 1 V		3		dB
V_{OFFSET} Input Range	Relative to ground		±2.5		V
V_{OFFSET} to V_{OUT} Gain			1		V/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−2.55		+2.7	V
Output Offset Voltage	V_{OFFSET} = 0 V, RTO	−10.9	+7	+18.7	mV
Output Offset Voltage Drift			−5.5		µV/°C
Short-Circuit Output Current			100		mA
POWER SUPPLY					
Operating Voltage Range		±4.5		±5.5	V
Quiescent Supply Current, I_{CC}/I_{EE}	@ ±5 V		+24/−21	+31/−27	mA
Supply Current Drift, I_{CC}/I_{EE}			+86/−77		µA/°C
+Power Supply Rejection Ratio (PSRR)	RTO	−48	−59		dB
−Power Supply Rejection Ratio (PSRR)	RTO	−48	−61		dB
TEMPERATURE RANGE		−40		+85	°C

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ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±5.5 V
Input Voltage	$\pm V_S$
V_{PEAK} and V_{GAIN} Control Pins	−3 V to $+V_S$
V_{OFFSET} Control Pins	$\pm V_S$
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead LFCSP	77	14	°C/W

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Maximum Power Dissipation

The maximum safe power dissipation in the AD8128 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8128. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface, which is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead LFCSP (48.5°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. Extra thermal relief is required for operation at high supply voltages.

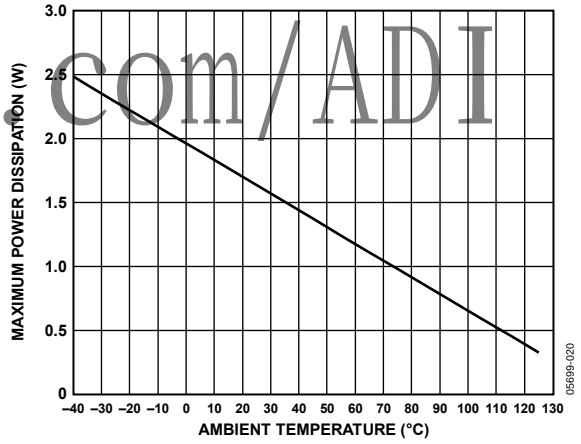

Figure 2. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

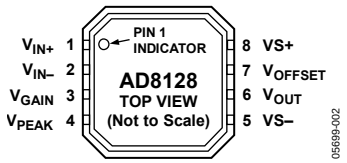

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{IN+}	Positive Equalizer Input
2	V_{IN-}	Negative Equalizer Input
3	V_{GAIN}	0 V to 1 V Broadband Gain Control
4	V_{PEAK}	0 V to 1 V High Frequency Gain Control
5	VS–	Negative Power Supply
6	V_{OUT}	Equalizer Output
7	V_{OFFSET}	DC Offset Adjust
8	VS+	Positive Power Supply
EP	GND	Ground Reference and Thermal Pad (see Exposed Pad (EP) section).

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TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Belden Cable, V_{OFFSET} = 0 V, unless otherwise noted.

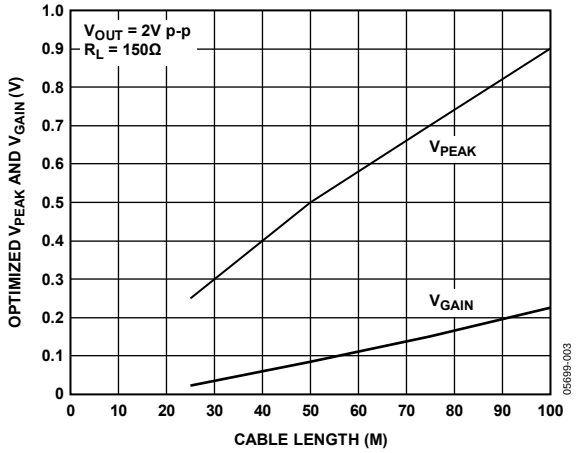

Figure 4. V_{PEAK} and V_{GAIN} Settings vs. Cable Length

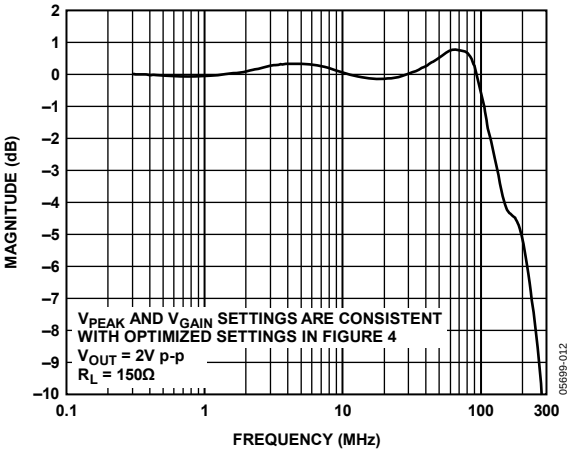
VPEAK AND VGAIN SETTINGS ARE CONSISTENT WITH OPTIMIZED SETTINGS IN FIGURE 4
VOUT = 2V p-p
RL = 150Ω
MAGNITUDE (dB)
FREQUENCY (MHz)
05699-012

Figure 7. Equalized Frequency Response for 50 M Cable

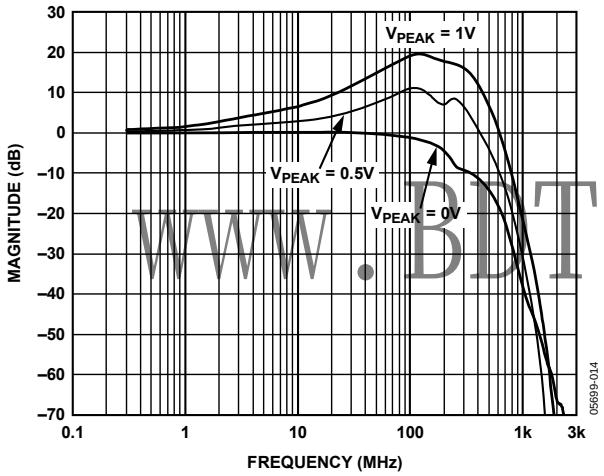

Figure 5. Frequency Response for Various V_{PEAK} Settings Without Cable

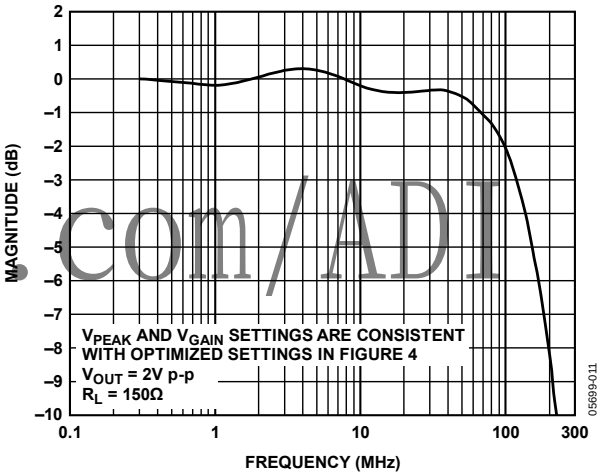
VPEAK AND VGAIN SETTINGS ARE CONSISTENT WITH OPTIMIZED SETTINGS IN FIGURE 4
VOUT = 2V p-p
RL = 150Ω
MAGNITUDE (dB)
FREQUENCY (MHz)
05699-011

Figure 8. Equalized Frequency Response for 100 M Cable

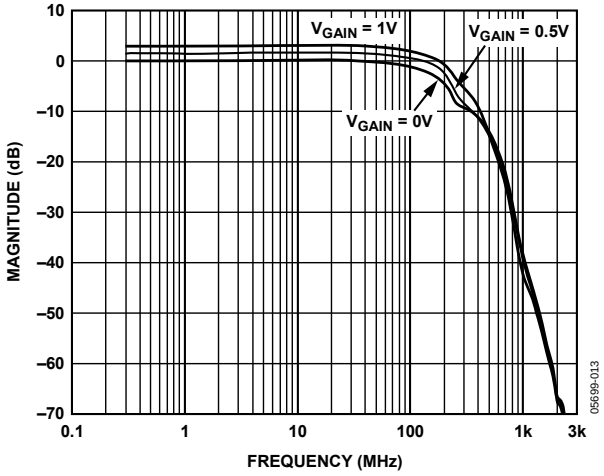

Figure 6. Frequency Response for Various V_{GAIN} Settings Without Cable

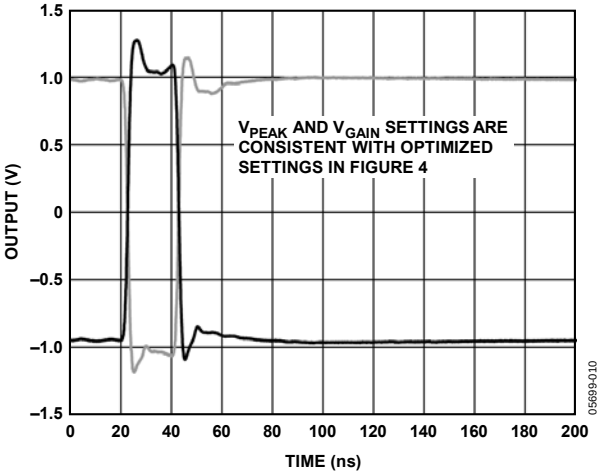

Figure 9. Equalized Pulse Response for 50 M of Cable

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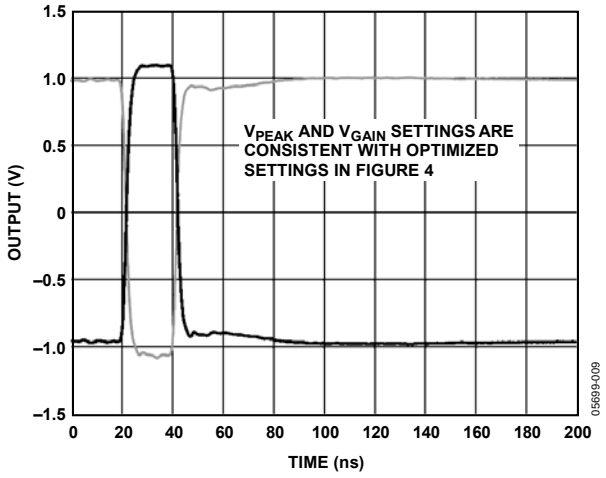

Figure 10. Equalized Pulse Response for 100 M of Cable

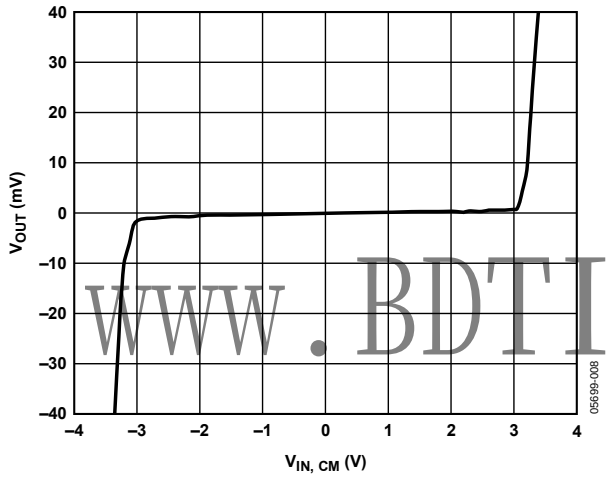

Figure 11. Output Voltage vs. Common-Mode Input Voltage

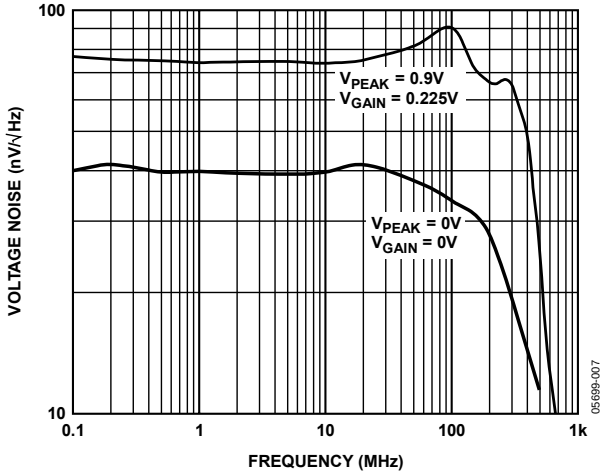

Figure 12. Voltage Noise vs. Frequency

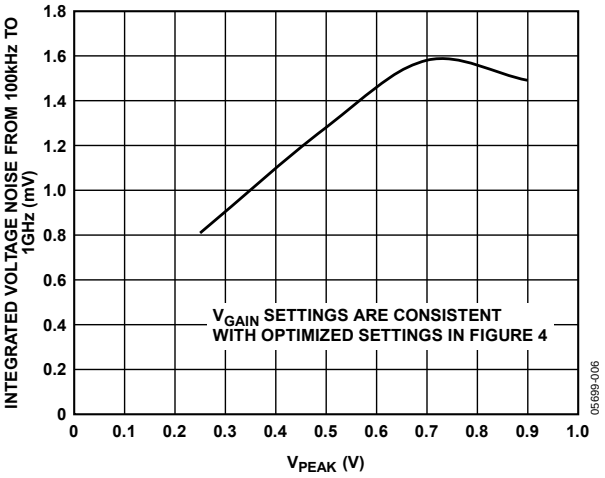
INTEGRATED VOLTAGE NOISE FROM 100kHz TO 1GHz (mV)
VGAIN SETTINGS ARE CONSISTENT WITH OPTIMIZED SETTINGS IN FIGURE 4
VPEAK (V)
05699-006

Figure 13. Integrated Voltage Noise vs. V_{PEAK}

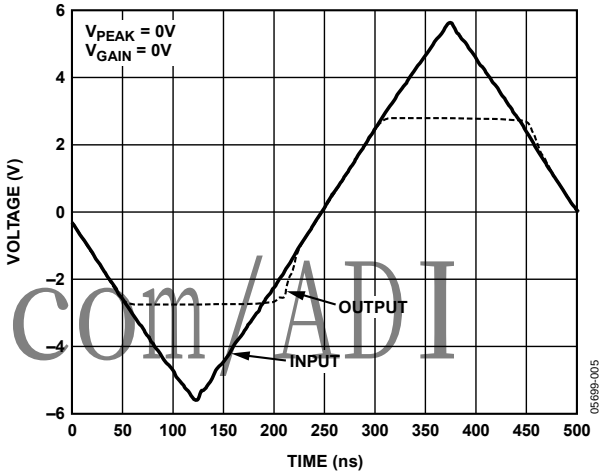

Figure 14. Overdrive Recovery Time

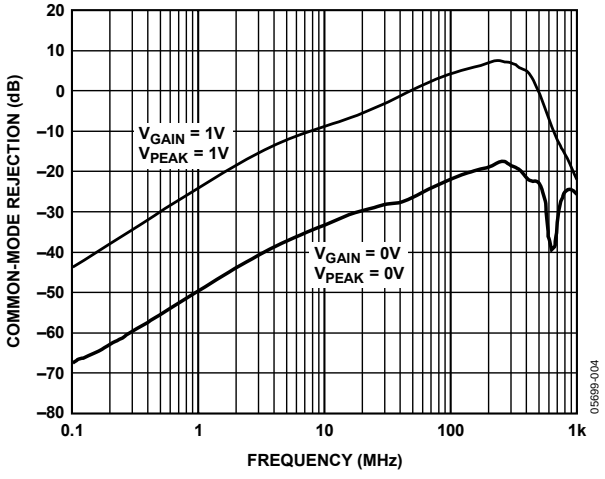

Figure 15. Common-Mode Rejection vs. Frequency

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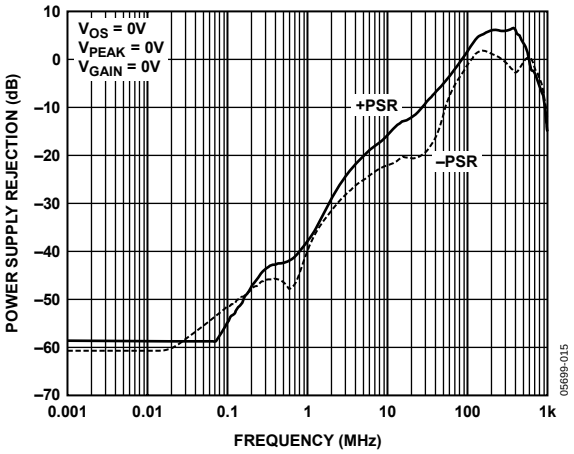

Figure 16. Power Supply Rejection vs. Frequency

TEST CIRCUIT

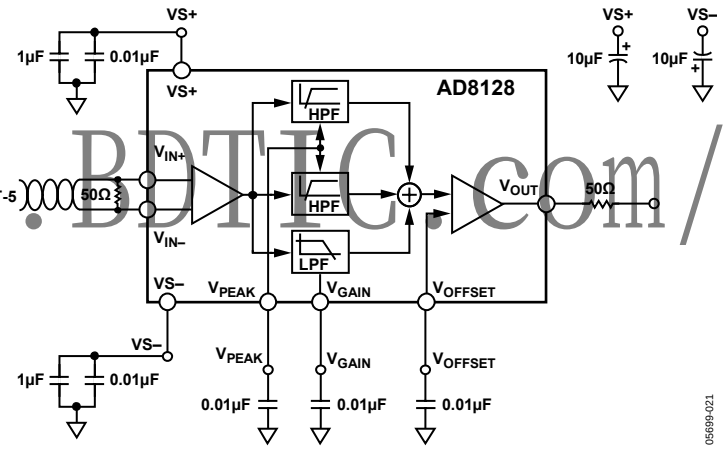

Figure 17.

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THEORY OF OPERATION

The AD8128 is a high speed, low noise analog line equalizer that compensates for losses in CAT-5/CAT-5e cables up to 100 meters with ±1 dB flatness in the pass band out to 70 MHz (see Figure 8). Two continuously adjustable control voltages alter the frequency response to add flexibility to the system by allowing for the compensation of various cable lengths as well as for variations in the cable itself. The dc control voltage pin V_{GAIN} adjusts ac broadband gain from 0 dB to 3 dB (see Figure 6) to account for dc resistive losses present in the cable. A second dc control voltage pin V_{PEAK} adjusts the amount of high frequency peaking (see Figure 5) from 0 dB to 20 dB. This compensates for the high frequency loss due to the skin effect of the cable.

The AD8128 has a high impedance differential input that allows it to receive dc-coupled signals directly from the cable. For systems with very high CMRR specifications, the AD8128 can also be used with a dedicated receiver, such as the AD8130 or AD8143, placed in front of it. The output of the AD8128 is low impedance and is capable of driving a 150 Ω load resistor and up to 20 pF of load capacitance at its output. For systems with high parasitic capacitances at the output, it is recommended that a small series resistor be placed between the output and capacitive load to reduce ringing in the pulse response.

The AD8128 is designed to be used in medium-length systems that have stringent low noise requirements as well as longer-length systems that can tolerate more noise. For the medium-length requirements, a single AD8128 is able to compensate up to 100 meters of cable with only 1.5 mV rms of output noise. For longer-length applications that require equalization of up to 200 meters of cable, two AD8128s can be cascaded together to achieve the desired equalization, while keeping approximately the same pass-band bandwidth, but with a slight degradation in settling time and slew rate.

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The frequency response of the AD8128 approximates the inverse frequency response of a lossy transmission line, which is given by

$$H(f) = e^{kl(1+j)\sqrt{f}} \quad (1)$$

where:

f is the frequency.

l is the length.

k is the line constant.

The AD8128 approximates the magnitude response of Equation 1 by summing multiple zero-poles pairs offset at different frequencies. Equalization adjustment due to varying line lengths is done by changing the weighting factors of each of the zero-pole pairs.

INPUT COMMON-MODE VOLTAGE RANGE CONSIDERATIONS

When using the AD8128 as a receiver, it is important to ensure that the input common-mode (CM) voltage range of the AD8128 stays within the specified range. The input CM level can be easily calculated by adding the CM level of the driver, the amplitude of any sync pulses, and the other possible induced common-mode signals from power lines and fluorescent lights.

$$V_{ICM} = V_{CM} + V_{SYNC} + V_{OTHER} \quad (2)$$

For example, when using a single 5 V supply on the drive side, the CM voltage of the line typically becomes the midsupply voltage, V_{CM} = 2.5 V. Furthermore, an addition of a sync signal, V_{SYNC} = 0.5 V, on to the common mode puts the peak CM voltage at 3 V. Assuming that both the driver and receiver have exactly the same ground potential, the signal is marginally below the upper end of the common-mode input range of 3.1 V. Other CM signals that can be picked up by the CAT-5 cable result in exceeding the CM input range of the AD8128.

The most effective way of not exceeding the CM level of the AD8128 is to lower the CM level on the driver. In the previous example, this was the primary contributor to the CM input level. If this is not possible, a dedicated receiver with a wider CM input range, such as the AD8130 or AD8143, should be used.

APPLICATIONS

KVM APPLICATIONS

In KVM applications, cable equalization typically occurs at the root of the KVM network. In a star configuration, a driver is located at each of the end nodes and a receiver/equalizer is located at the single root node. In a daisy-chain configuration, each of the end nodes are connected to one another, and one of them is connected to the root. Similarly, the drivers are placed on the nodes, and the receivers/equalizers are placed at the root.

In both of these aforementioned configurations, three AD8128 receiver/equalizers can be used at the root node to equalize the transmitted red (R), green (G), and blue (B) channels for up to 100 meters of cable. Since the skew between two pairs of cables in CAT-5 is less than 1%, the control pins can be tied together and used as a single set of controls.

If the common-mode levels of the inputs permit using the AD8128 as a receiver (see the Input Common-Mode Voltage Range Considerations section), the input signal should be terminated by a 100 Ω shunt resistor between the pairs, or by two 50 Ω shunt resistors with a common-mode tap in the middle. This CM tap can be used to extract the sync information from the signal if sync-on-common-mode is used.

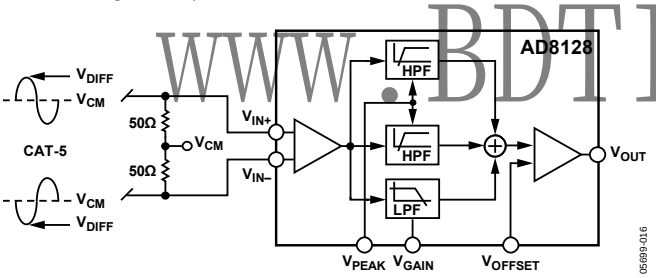

Figure 18. Single Receiver Configuration for CAT-5 Equalizer

DC CONTROL PINS

The AD8128 uses two control pins (V_{GAIN} and V_{PEAK}) to adjust the equalization based on the length of the cable and one pin (V_{OFFSET}) to adjust the dc output offset. V_{GAIN} is a user-adjustable 0 V to 1 V broadband gain control pin, and V_{PEAK} is a 0 V to 1 V adjustable high frequency gain pin to equalize for the skin effect in CAT-5 cable. The values of both V_{PEAK} and V_{GAIN} are linearly correlated to the length of the cable to be equalized. A simple formula can be used to approximate the desired values for both of these pins.

$$V_{GAIN} = \frac{length(m)}{425\text{m/V}} \quad (3)$$

$$V_{PEAK} = \frac{length(m)}{110\text{m/V}} \quad (4)$$

While these equations give a close approximation of the desired value for each pin, to achieve optimal performance, it may be necessary to adjust these values slightly.

Figure 19 and Figure 20 illustrate circuits used to adjust the control pins on the AD8128. In Figure 19, a 1 kΩ potentiometer is used to adjust the control pin voltage between the specified range of 0 V to 1 V. In Figure 20, a 2 kΩ potentiometer is used to control the offset pin from −2.5 V to +2.5 V. For both of these configurations, a ±5V supply is assumed.

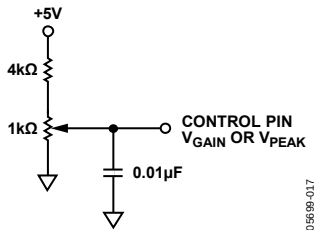

Figure 19. Circuit to Control V_{GAIN} and V_{PEAK} (0 V to 1 V)

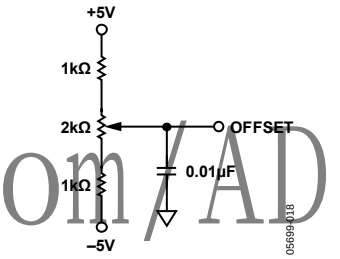

Figure 20. Circuit to Control V_{OFFSET} (±2.5 V)

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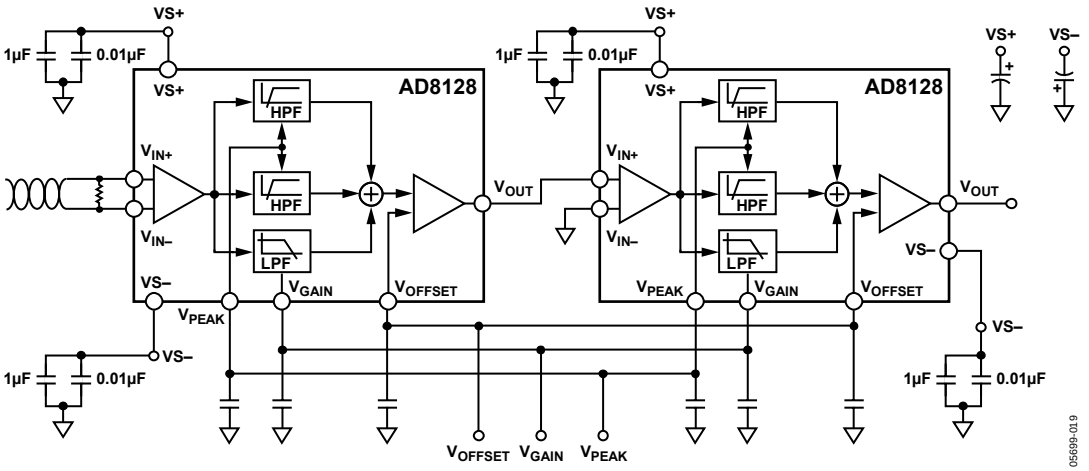

Figure 21. Cascaded AD8128 Configuration

CASCADED APPLICATIONS

To equalize distances longer than the specified 100 meters, the AD8128 can be cascaded to provide equalization for longer distances. When combining two AD8128s in series, it is possible to link the control pins together and use them like a single control pin for up to 200 meters of equalization.

In this configuration, it is important to note that some key video specifications can be slightly degraded. By combining two equalizers in series, specifications such as rise time and settling time both increase while 3 dB bandwidth decreases slightly. Also, integrated noise is increased because the second equalizer adds gain. Subjective testing should be done to determine the appropriate setting for the three control pins for optimum equalization.

EXPOSED PAD (EP)

The 8-lead LFCSP has an exposed paddle on the underside of its body. To achieve the specified thermal resistance, it must have a good thermal connection to one of the PCB planes. The exposed paddle must be soldered to a pad on top of the board connected to an inner plane with several thermal vias. For the AD8128, this pad must also be electrically connected to ground to provide a ground reference to the part.

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the AD8128. A solid ground plane is recommended and good wideband power supply decoupling networks should be placed as close as possible to the supply pins and control pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

EVALUATION BOARDS

There are two evaluation boards available for easy characterization of the AD8128. A general-purpose evaluation board consisting of a single AD8128, with an option of also using a dedicated receiver, is available for simple characterization of the part. Additionally, a KVM application specific evaluation board is available. This evaluation board consists of six AD8128s to equalize each of the RGB channels up to 200 meters, a 16-pin 26C32 comparator for sync-on-common-mode extract and a triple op amp to provide additional gain if necessary.

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OUTLINE DIMENSIONS

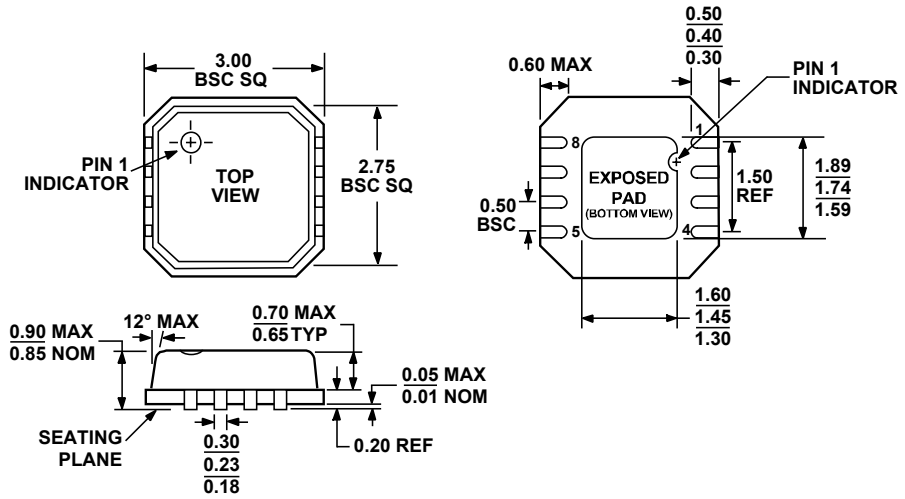

Figure 22. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

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Model	Temperature Range	Package Description	Package Option	Branding
AD8128ACPZ-R2	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HZB
AD8128ACPZ-RL[1]	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HZB
AD8128ACPZ-R7[1]	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package (LFCSP_VD)	CP-8-2	HZB

[1] Z = Pb-free part.

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